UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,226	04/18/2001	Kevin John Moore	169.2025	6435

5514 7590 10/19/2004

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
WOODS, ERIC V	
ART UNIT	**PAPER NUMBER**
2675	8

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,226	MOORE, KEVIN JOHN	
	Examiner	Art Unit	
	Eric V Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *29 September 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. A substitute specification covering the claims is required pursuant to 37 CFR 1.125(a) because the terms used omit essential subject matter and use terminology not conventionally accepted in the art.

A substitute specification must not contain new matter. The substitute specification must be submitted with markings showing all the changes relative to the immediate prior version of the specification of record. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strike-through cannot be easily perceived. An accompanying clean version (without markings) and a statement that the substitute specification

contains no new matter must also be supplied. Numbering the paragraphs of the specification of record is not considered a change that must be shown.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> **Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.**

5. Claims 1-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Namely, the claims are directed to an algorithm that a human being of ordinary skill in the art could perform using pencil and paper, thus being both abstract subject matter and lacking utility (see MPEP 2111 [R-1]). Furthermore, although applicant mentions that such implementations could be done using integrated circuits or hardware, applicant does not limit these claims to execution on or by a computer. Therefore, the claims are to a mathematical algorithm and are not patentable.

6. To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

8. Claim 1-6, 12-17, and 23-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. That is, applicant uses the term 'directed adjacency graph' as central to all the claims and in the specification. However, according to every conventional definition in graph theory, for example the NIST website, makes it clear that a tree, by definition, is an **undirected** acyclic graph. However, applicant in claim 5 specifies that a "directed adjacency graph" can be an expression tree (this is an evidence claim). Applicant has defined an expression tree in the specification to be a binary-type tree. Therefore, the claim language contradicts the use of the term "directed". Furthermore, the term "adjacency graph" is redundant and repetitive, as a graph is universally accepted to be composed of a set of edges E and a set of vertices or nodes V or N. Therefore, any kind of graph (undirected, cyclical, etc.) could be taken as the target of the invention and as the entire invention revolves around the use of "directed adjacency graphs", revision is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 7–11, 18-22, and 29-33 are rejected 35 U.S.C. 102(a) as being anticipated by Fraser *et al* (AU 9947508 A), which has a publication date older than the filing date of the Australian application for which priority is claimed.

As to claims 7 and 18, reference Fraser teaches all the limitations. Expression trees are discussed and all the requirements of the preamble met (see pg. 45, lines 10-26; pg. 46, lines 1-5). Fraser teaches the selection of a region of pixels and their use as a leaf node-primitive and the use of an operator as a parent node (see pg. 45, lines 10-26; pg. 46, lines 1-5). Further, all the cases of active and inactive nodes are covered (see pg. 45, lines 23-26). The process of traversing the nodes, setting active flags, and similar is all covered in pages 47-50 of the Fraser specification. Furthermore, Fraser teaches the generating of operator instructions (see pg. 30, lines 14-2).

As to claims 8 and 19, reference Fraser teaches all the limitations. Again, see the above discussion about Fraser (see pgs. 47-50).

As to claims 9 and 20, reference Fraser teaches all the limitations. Fraser teaches a method of processing graphical objects to form a raster pixel image on both one and a subsequent scan line, meeting the recited requirement of a plurality of pixel locations and a plurality of scan lines (see col. 4, lines 8-26). The use of expression trees and their details are discussed in the rejections for claims 7 and 8 above. Again, such a tree is shown in Fig. 19 with binary nodes, a plurality of leaf nodes, and the other required elements. As to the method claims, see below.

In Figs. 20A-20C, there is clearly illustrated a table that represents an expression tree. This table is clearly defined in terms of union regions, e.g. the areas of each pixel

that overlap and that has active fields. Further, each row represents an entry in the table representing a binary or leaf node. The table clearly shows that each record has both first and second fields that show whether a left or a right node is required for an operation. This is evident in both the data_in_SΠD fields and the multiple _Active fields. Next, the third and fourth fields that indicate whether the left or right nodes are active are a combination of Src_Active, and one of data_in_SΠD fields.

Fraser teaches the determining of pixel locations (see col. 3, lines 23-40). The traversing and generating steps are discussed in the rejections for claims 7 and 8 under Fraser. Finally, Fraser teaches the execution of the instruction to render the image from the image-rendering apparatus 20 (see Fig. 3, the output 898 from the pixel output module 800 that does the rendering, and the entire rendering apparatus 20).

As to claims 10 and 21, reference Fraser teaches multiple fields in the table representing the binary elements of the expression tree as discussed in the above rejection. However, there are other fields besides the four discussed above that are disclosed in Figs. 20A-20C. While the fields are not explicitly directed to holding the information on overlap in the common area, the nature of the fields should be taken into account here. The phrasing "data_in_SΠD fields" that is utilized by Fraser in his description of the invention is such that it accommodates overlap because it represents set relationships. If there were overlap between source and destination, it would be indicated in these fields. Therefore, it would be valid to hold that these and the other fields inherently hold this information and thus would meet the requirements recited by

the claim. All of the traversal requirements and subsequent portions of the claim are discussed above for claim 9.

As to claims 11 and 22, reference Fraser teaches that these tables are used to implement clipping operations, particularly the tables shown in Figs. 27B and 29A, including the CLIP_IN and CLIP_OUT operations, specifically a clip-type flag (see col. 22, lines 20-45, regarding omitted flags that would be transferred to the level and/or activity tables). That is, the level and activity tables discussed in Fraser could be combined as shown in Figs. 20G-20I in discussing alternative implementations. Thusly, the flags discussed as missing from Fig. 15 would be present and allow the fulfilling of the recited requirements of the claim (see col. 22, lines 20-45).

As to claims 29-33, they are rejected as above, e.g. please see:

-Claims 7 and 18 for claim 29 rejection;

-Claims 8 and 19 for claim 30 rejection;

-Claims 9 and 20 for claim 31 rejection;

-Claims 10 and 21 for claim 32 rejection;

-Claims 11 and 22 for claim 33 rejection.

Fraser teaches the additional limitation of computer-readable media (pg. 15, lines 25-31; pg. 16, lines 1-4).

11. Claims 7-8, 18-19, and 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Politis (US 5,754,121).

As to claims 7, 18, and 29, reference Politis discloses the use of expression trees (see col. 8, lines 16-40). Furthermore, the "expression trees" shown in Figures 16-18

are binary; that is, as evinced in Figs. 17 and 18 particularly, each parent node has both a left and a right descendent node, which each consist of a graphical object. The parent node is an operator, representing a common, overlapping region, e.g. nodes 37, 36, and 26 on Fig. 17, and the descendent nodes represent graphical objects, e.g. nodes 28-30 and others on Fig. 17. Next, Politis teaches that these trees are decomposed into lower-level instructions (see col. 4, lines 3-8). Politis teaches these graphs as trees, but (see Figs. 7, 8, 16, and others) they have leaf nodes (see col. 11, lines 30-33) and parents (see col. 14, lines 25-32). Examiner interprets these terms, e.g. leaf and parent nodes, to have the normal meanings associated with them in graph theory. The parent nodes are found to be operators (element 26, Fig. 17) as shown in Figs. 16, 17, and 18 (see col. 13, lines 33-60). The leaf or descendent nodes are shown in the above figures (elements 20, 24, etc.) and are representing graphical objects such as letters (see col. 13, lines 33-60). Therefore, all the recited portions of the preamble to claim 7 are met. Rejection of the method steps follows below.

Reference Politis teaches that there are separate groups of pixel locations determined (see col. 4, lines 15-32), and such selections are illustrated in Figs. 30 – 32, as regions of pixels are shown with their bounding boxes (see col. 11, lines 3-4). Furthermore, the operators are all described as operating within a region limited by such a box (see col. 11, lines 3-4). The selection of active or inactive regions is clearly shown in Fig. 17 as graphical regions are selected and would *prima facie* pass information up the tree or graph containing them. Also, Politis very clearly teaches the determining of active pixel areas (col. 9, lines 31-42) and the updating of it – that is,

inactive or completed instructions are pruned from the list. Only the active leaf nodes would be placed into the active list for a given location during the drawing process - that is, as the rasterizing shifted, the active instruction pool would update. Again, the above means that the tree is traversed as the rasterizing / scanning process occurs; the instructions are generated and put into the active list (see col. 9, 12-25 and 31-52). Furthermore, the tree is traversed recursively, thusly all the nodes are determined active or not – since the traversal is done immediately before execution to save memory, this means that it is constantly traversed to determine active and inactive nodes for compile-time and real-time optimization (see col. 8, lines 15-40).

The order of traversal of the nodes, which is explicitly recited in claim 7, corresponds to the preorder traversal taught by Politis (see col. 14, lines 25-55). The generation step for the trees is described in the lines referenced above, e.g. the trees are constructed during each line scan. For further exploration of the issues not explicitly discussed here, please see the below rejection under U.S.C. 103 in the Politis section.

As to claims 8, 19, and 30, which focus only on the details of traversing the expression tree of claim 7, the refutation of the expression tree traversal paths based on Politis as above shows that Politis teaches all these limitations, including the additional limitation of computer-readable media met by claim 23 of Politis (see col. 25, lines 34-35).

12. Claims 7-8 and 18-19 are both rejected under 35 U.S.C. 102(b) as being anticipated by a mental process and pencil and paper, e.g. the applicant is claiming methods of traversing a tree composed of graphical objects that can be performed by

hand by a person – see MPEP 2111 [R-1]. This claim would cover the drawing of graphical trees for educational and instructional purposes, particularly computer programming, where such activity is practiced on a regular basis. Furthermore, the applicant has not limited these claims to execution on or by a computer, and such claims must be read as broadly as possibly – see MPEP 2111 [R-1].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

14. Claims 1-6, 12-17, and 23-28 are rejected under 35 U.S.C. 103(a) as being anticipated by Politis in view of Katzenberger (US 5,970,496). Please note: claims 12-17 are treated with 1-6, as 12-17 are the apparatus implementing 1-6; claims 23-28 are referenced to 1-6 and 12-17 with the additional limitation of computer-readable media covered beforehand.

As to claims 1 and 12, reference Politis discloses the use of expression trees (see col. 8, lines 16-40). Furthermore, the "expression trees" shown in Figures 16-18 are valid forms of trees, which are by definition undirected acyclic graphs. Next, Politis teaches that these trees are decomposed into lower-level instructions (see col. 4, lines 3-8). Politis teaches these graphs as trees, but (see Figs. 7, 8, 16, and others) they have leaf nodes (see col. 11, lines 30-33) and parents (see col. 14, lines 25-32). The parent nodes are found to be operators (element 26, Fig. 17) as shown in Figs. 16, 17,

and 18 (see col. 13, lines 33-60). The leaf or descendent nodes are shown in the above figures (elements 20, 24, etc.) and are representing graphical objects such as letters (see col. 13, lines 33-60). Therefore, all the recited portions of the preamble to claim 1 and 12 are met. Rejection of the method steps follows below.

Reference Politis teaches that there are separate groups of pixel locations determined (see col. 4, lines 15-32), and such selections are illustrated in Figs. 30 – 32, as regions of pixels are shown with their bounding boxes (see col. 11, lines 3-4). Furthermore, the operators are all described as operating within a region limited by such a box (see col. 11, lines 3-4). The claim recites, "...wherein the said portion of the directed adjacency graph is that portion which passes data up the directed adjacency graph..." (Ellipses added). This language is with used with respect to the determining of the graph to be operated upon, which is clearly shown in Fig. 17 as graphical regions are selected and would *prima facie* pass information up the tree or graph containing them. Also, Politis very clearly teaches the determining of active pixel areas (col. 9, lines 31-42) and the updating of it – that is, inactive or completed instructions are pruned from the list. Only the active leaf nodes would be placed into the active list for a given location during the drawing process - that is, as the rastering shifted, the active instruction pool would update. Again, the above means that the tree is traversed as the rasterizing / scanning process occurs; the instructions are generated and put into the active list (see col. 9, 12-25 and 31-52). Lastly, the generation step for the trees is described in the lines referenced above, e.g. the trees are constructed during each line scan.

Reference Katzenberger discloses the use of directed acyclic graphs to store graphical information in Figs. 2 and 4B, particularly Fig. 4B (see col. 1, lines 9-11). Parent and child nodes are used in this invention (see col. 2, lines 53-65); child nodes are the same thing as the "leaf" nodes referenced by applicant (see col. 1, lines 55-65). Furthermore, Katzenberger teaches the use of operators for performing operations on graphical areas – Fig. 14 shows the use of various operators such as 'cno' and 'ctg' that meet the requirement of the claim, even if they primarily emphasize the data relationships. As seen in Fig. 4B, Katzenberger shows the simplest graphical elements as the leaf nodes. Therefore, it would be obvious to one of ordinary skill in the art to combine the instruction trees of Politis with the graph structures of Katzenberger. The motivation would be to allow compiler-style optimization of rasterizing instructions and to enable the effective use of directed acyclic graphs as discussed by Politis (see Politis col. 10, lines 1-11 and 37-40) and also to derive the benefits of the DAG storage structures as shown by Katzenberger in those figures referenced above.

As to claims 2 and 13, references Politis and Katzenberger teach all the limitations. Reference Katzenberger teaches a table for storing graphical instructions for acting on image components in Fig. 9, thus meeting the details recited in claim 2. See claim 1 for motivation and combination.

As to claims 3 and 14, references Politis and Katzenberger teach all the limitations. Reference Politis teaches the use of a "Cliplist" in Fig. 24 that contains a listing of elements to be moved. This list is stored in a one-column tabular format as shown in the Figure, and an operator does perform this action (see col. 3, lines 20-40).

This data is constructed as the tree is traversed and could easily be inserted into the table of Katzenberger shown in Fig. 9. See claim 1 for motivation and combination.

As to claims 4 and 15, reference Katzenberger discusses traversing a directed acyclic graph (see col. 18, lines 8-15). This step is executed as part of an operation on the data structure. As discussed in claim 1, the active nodes are read in for each pass and updated, therefore both the operators and the active leaf nodes are traversed and translated into instructions, thus meeting the requirements of the claim. See claim 1 for motivation and combination.

As to claims 5 and 16, reference Politis discloses the use of expression trees (see col. 8, lines 16-40). Furthermore, the "expression trees" shown in Figures 16-18 are valid forms of trees, which are by definition undirected acyclic graphs. Next, Politis teaches that these trees are decomposed into lower-level instructions (see col. 4, lines 3-8). Politis teaches these graphs as trees, but (see Figs. 7, 8, 16, and others) they have leaf nodes (see col. 11, lines 30-33) and parents (see col. 14, lines 25-32). Examiner interprets these terms, e.g. leaf and parent nodes, to have the normal meanings associated with them in graph theory. The parent nodes are found to be operators (element 26, Fig. 17) as shown in Figs. 16, 17, and 18 (see col. 13, lines 33-60). The leaf or descendent nodes are shown in the above figures (elements 20, 24, etc.) and are representing graphical objects such as letters (see col. 13, lines 33-60). Therefore, it would be obvious to one of ordinary skill in the art to combine the trees of Politis with the graphic forms of Katzenberger. The motivation would be to have a tree structure to optimize as per claim 1 (see claim 1 references and col. 4, lines 1-10).

As to claims 6 and 17, reference Politis teaches the use of binary operators on the expression trees – see Figs. 28-29, for example. See claim 1 for combination and motivation.

As to claims 23-28, they are rejected as above with the additional limitation of computer-readable media met by claim 23 of Politis (see col. 25, lines 34-35), e.g. please see:

-Claims 1 and 12 for claim 23 rejection;

-Claims 2 and 13 for claim 24 rejection;

-Claims 3 and 14 for claim 25 rejection;

-Claims 4 and 15 for claim 26 rejection;

-Claims 5 and 16 for claim 27 rejection;

-Claims 6 and 17 for claim 28 rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V Woods whose telephone number is 703-308-0000 (phone not yet installed, please call receptionist at 703-305-3900). The examiner can normally be reached on M-F 7:30-5:00 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Woods
September 29, 2004

JEFFERY BRIER
PRIMARY EXAMINER